

## Design Rules Verification Report

Filename : C:\Users\Peep\Documents\SVN\Trinamic-TMC846x\TMC-8461-R8\TMC8461-E  
VAL-V3.0.PcbDoc

Warnings 0  
Rule Violations 1

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.15mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ( All )	1
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.15mm) (Max =2mm) (Preferred=0.2mm) (All)	0
Routing Via (MinHoleWidth=0.2mm) (Max HoleWidth=0.6mm) (PreferredHoleWidth=0.25mm) (MinWidth=0.5mm)	0
Power Plane Connect Rule(Relief Connect )(Expansion=0.4mm) (Conductor Width=0.2mm) (Air Gap=0.2mm)	0
Minimum Annular Ring (Minimum=0.124mm) (((ObjectKind = 'Pad') OR (ObjectKind = 'Via')) And (Layer = 'MultiLayer'))	0
Minimum Annular Ring (Minimum=0.15mm) (((ObjectKind = 'Pad') OR (ObjectKind = 'Via')) And (Layer = 'MultiLayer'))	0
Hole Size Constraint (Min=0.2mm) (Max=6mm) (All)	0
Net Antennae (Tolerance=0mm) (All)	0
Component Clearance Constraint ( Horizontal Gap = 0mm, Vertical Gap = 0mm ) (All),(All)	0
Height Constraint (Min=0mm) (Max=40mm) (Preferred=12.5mm) (All)	0
Total	1

Un-Routed Net Constraint ( All )	
Un-Routed Net Constraint: Net +3V3 Between Track (18.83mm,41.71mm)(20.06mm,41.71mm) on Mid1 And Track	